Micron qHD FLCOS Microdisplay Panel

MT7DPQHBCBBA-A1

Features

- Fast switching ferroelectric liquid crystal (FLC) material eliminates motion smearing
- Supports full consumer-product temperature ranges with integrated temperature compensation
- All digital pixel architecture provides superior image quality
- Flexible video interface is easily adapted to most digital video sources
- Adjustable color field durations
- 50/60Hz frame rate (300/360Hz RGB field rate)

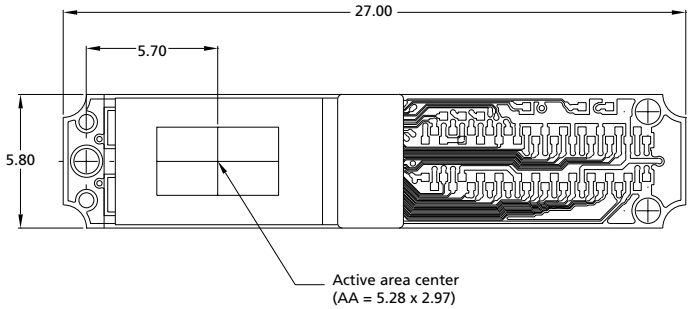
Supported Interfaces

- 24-bit RGB parallel data, Hsync, Vsync, Valid, Clock
- 24-bit YCrCb 4:4:4 data, Hsync, Vsync, Valid, Clock
- 16-bit YCrCb 4:2:2 data, Hsync, Vsync, Valid, Clock
- Industry-standard two-wire bidirectional serial

Optical

- Color-sequential operation
- Zero-count stuck white pixels
- Reflectivity: 58%
- 300:1 contrast ratio

Figure 1: Panel Illustration



Electrical Interface

- Fully integrated display controller requires no additional circuitry to interface with digital video input signals
- Supports PAL and NTSC
- Programmable video cropping and downscaling
- Programmable color matrix processor
- Embedded LED driver controller with adjustable color field durations
- Adjustable gamma settings

Table 1: Key Specifications

Format	qHD: 960 x 540 full-color pixels
Active area diagonal	6.06mm (0.24-inch)
Color depth	24-bit RGB
Contrast ratio	300:1
Power consumption	160mW (display panel + integrated controller)
Operating temperature	–10°C to +70°C
Package	27.0mm x 5.8mm x 2.7mm (W x H x D)

Contents

List of Figures

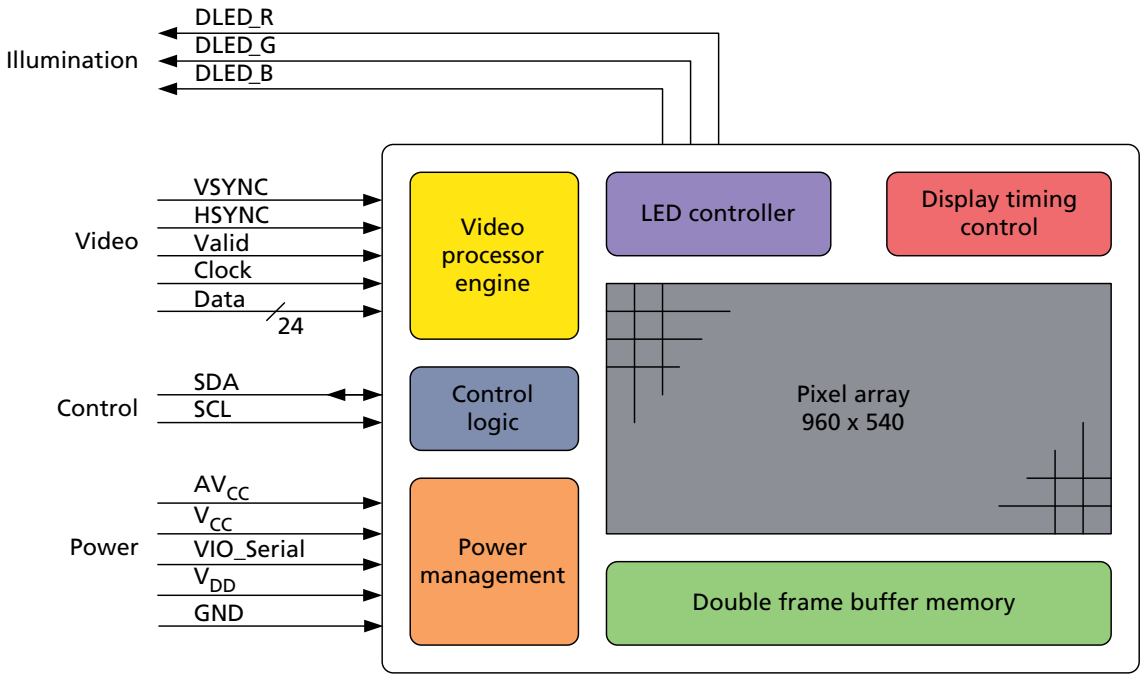
List of Tables

Introduction

This data sheet provides a detailed technical description of the qHD display panel and offers the information required to integrate this panel into a display system. The display panel is designed to be combined with an illumination source, polarizing optics, and a lens to create a complete display solution.

This product takes advantage of the fast switching speeds and superior optical qualities of patented Ferroelectric Liquid Crystal (FLC) materials, delivering high-quality images free of motion smearing. Using a color sequential mode of operation, the product is capable of showing up to 16.777 million colors when combined with an RGB illumination source. This product is an integrated FLCOS solution, providing standard digital interfaces for an easily integrated, high-performance solution that does not require any additional support components.

Figure 2: Block Diagram of the Display Panel



Display Panel Overview

The display panel provides a compact solution for converting electronic video data into full-color and high-quality live images. When polarized light is directed towards the display panel, the light reflected from the display panel makes up gray scale images when viewed through a crossed polarizer and lens system. A schematic drawing of an example projection display system is shown in Figure 3 (page 7). In the figure, sequential red, green, and blue light from an RGB illumination source is polarized and reflected by a polarizing beam splitter (PBS) onto the display panel. The light also passes through pre-polarizing, beam shaping, and homogenization optics to avoid stray light of unwanted polarization and to create an even illumination of the display panel.

The display panel consists of a reflective silicon backplane, a layer of ferroelectric liquid crystal, and a glass cover—all of which are mounted in a miniature electro-optic package. Through a connector located on the rear of the package, video data is fed to the silicon backplane controlling the voltage applied to its top reflective and pixelated surface. The voltage applied to each pixel determines the orientation of the liquid crystal molecules, which in turn determines the polarization state of the light reflected from each pixel of the display panel. The video data is used to control the time that each pixel is in particular polarization states (for example, pulse width modulation). A cross-polarizer or polarizing beam splitter will only transmit one type of polarization, thereby creating gray scale pixels according to the voltage that was applied to the pixels and the time spent in each state. The light transmitted through the polarizing beam splitter is typically captured by a lens system magnifying the image before it reaches the observer.

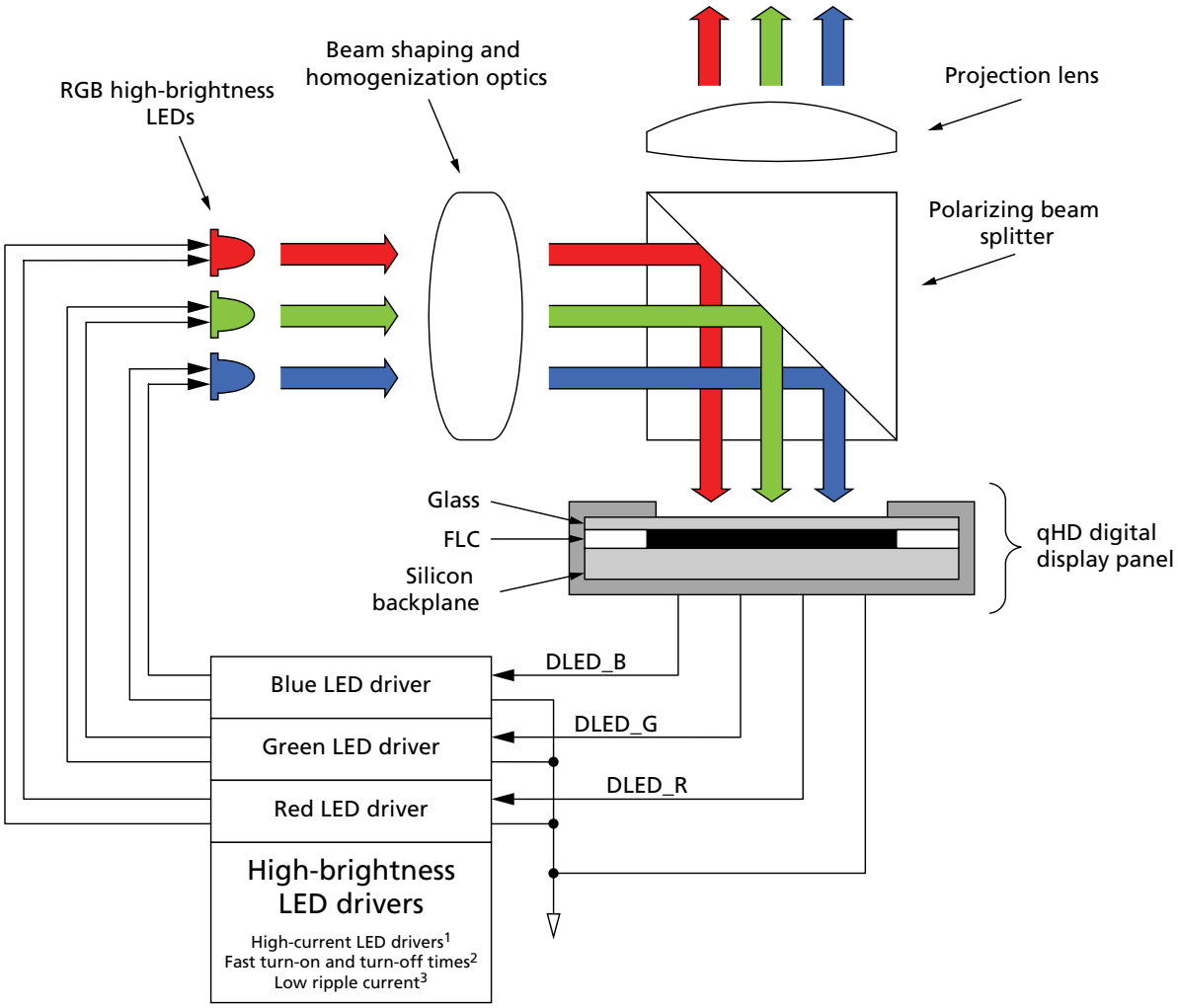
The display panel works in a color sequential mode, which means that the image data for the colors red, green, and blue are shown as three separate image fields in time. The human eye then integrates the three individual gray scale color images to produce the intended image with final color. To achieve this, the light source only emits one color at a time, and during that time the corresponding image data is shown on the display backplane. This is done at a very high frequency in the display panel—typically at 360Hz (color field rate).

The silicon backplane contains all of the necessary circuits to receive a standard 24-bit parallel RGB progressive raster scan video image and generate the voltages and timing commands for each pixel. Dual frame memory buffers are embedded in the silicon. The backplane includes additional circuits to facilitate easy system integration and customization, such as video scaling, video cropping, gamma correction, and color correction circuits. The backplane generates three discrete digital signals to instruct the illumination system when to illuminate the panel with each color of polarized light. The duration of each color's ON time period can be adjusted to allow for system optimization.

Table 2: Operating and Environmental Specifications

Item	Min	Typ	Max	Unit
Operating temperature (panel temperature)	–10	27	70	°C
Storage temperature	–30	–	80	°C

Figure 3: Example of a MT7DPQHBCBBA-A1 Projector Application



Notes:
1. Current levels are application dependent.
2. LED drivers must be able to provide and remove current quickly; turn-on and turn-off times should remain below 5µs.
3. For best visual results, the ripple current should remain below 10%.

Optical Specification

The display panel is intended to be one part of an optical system consisting of this display panel, an RGB illumination source, polarization optics, and magnification optics. In combination, these optical components create a display system with quantifiable optical properties. The display panel's optical performance is specified for use in an optical system that approximates a consumer display application (mechanically aligned panel, f/2.4, and telecentric optics). For best performance, the polarizing optics must be aligned with the columns of the display panel.

The display panel's active array pixels are surrounded by additional pixels, which are then surrounded by a pixelated common electrode. These additional pixels and the common electrode are driven so as to create the appearance of a black surround to the displayed image. Defective pixels (stuck on) and/or other artifacts may appear in these additional regions. It is recommended that the optics system take care to aperture the light reflecting to and from these regions.

Table 3: Optical Specifications

Item	Min	Typ	Max	Unit
Active area resolution		960 x 540		pixels
Active area size		5.28 x 2.97		mm
Pixel pitch		5.5 x 5.5		µm
Fill factor	–	86	–	%
Contrast ratio (under typical operating conditions)	–	300:1	–	
Reflectivity (On-state photopic transmission through a crossed polarizer)	–	58	–	%
Transmission uniformity (On-state)	80	–	–	%

Note: 1. Typical values at 60Hz NTSC (gamma correction of 2.1), 24-bit RGB operation video pattern at room temperature.

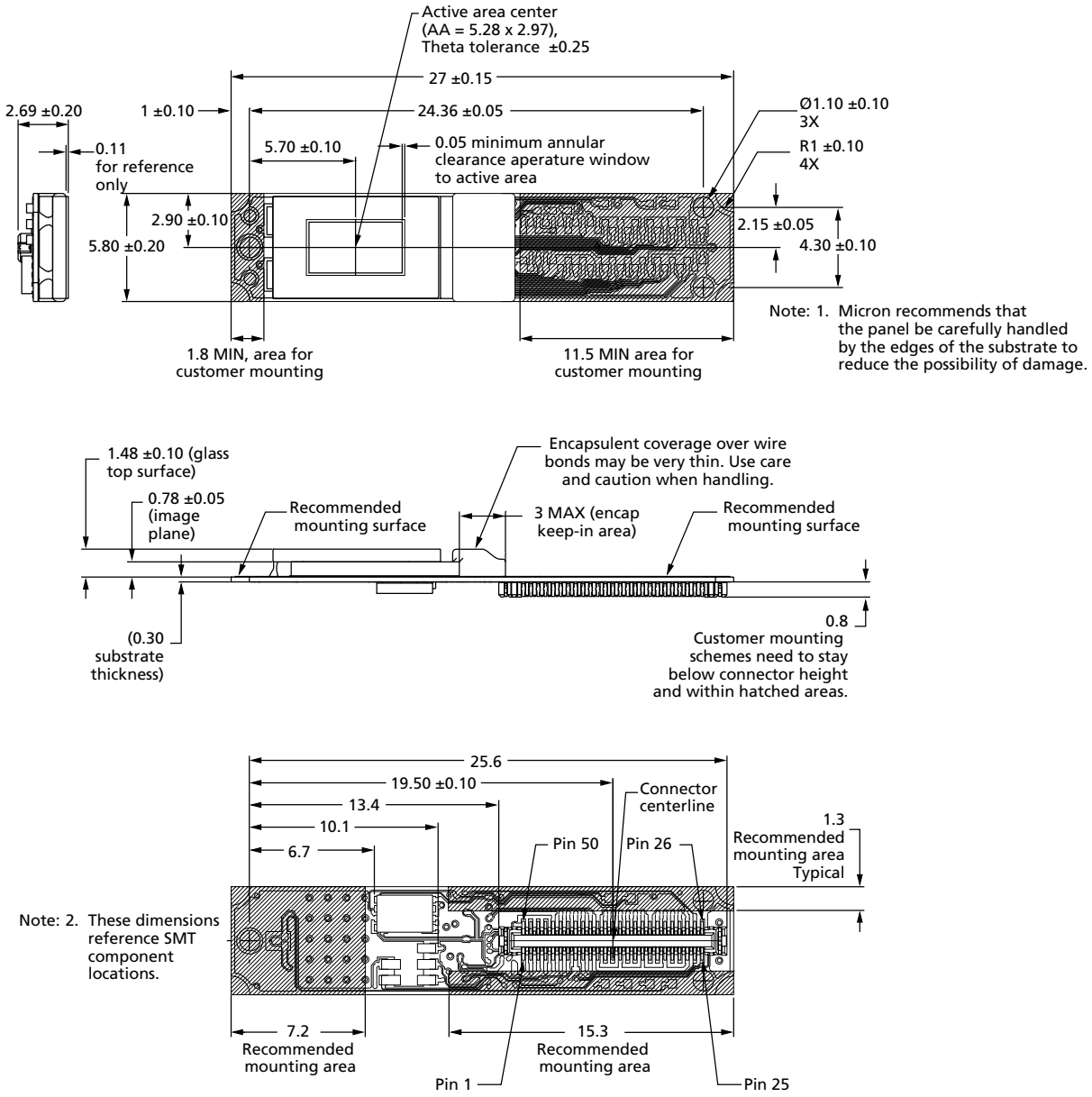
Mechanical Specifications

This display panel is an LCOS cell mounted onto a BT substrate. A 50-pin, 0.4mm pitch, board-to-board connector is located on the back of the BT substrate, which allows for electrical interconnection. The display panel uses connector part number Molex 502430-5010.

The display panel weighs 0.35 grams.

Liquid crystal displays are sensitive to mechanical stress. This package is designed to isolate mounting forces from the display panel. Care must be taken to prevent torsion of the BT substrate. No force may be applied directly to the actual LCOS cell. The unit should be mounted into position using the BT substrate area outside and away from the LCOS cell. The area behind the connector must be supported to avoid the torsion of the BT substrate during connector mating. The 1.10mm diameter locating holes may be used to mount the unit by means of heat-staked or swage-locked pins that do not add mechanical stress to the package; however, plastic clips, brackets, or other similar mounting schemes are recommended. It is also recommended that the unit be mounted to plastic or other dielectric type material surfaces to avoid electrical shorting with circuitry on the BT substrate.

Figure 4: Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Tolerances are ±0.1mm (±.004in) unless specified otherwise.

Display Panel Interface Electrical Specifications

The display panel is an LCOS microdisplay, consisting of a CMOS integrated circuit. This IC acts as a combined controller and display driver circuit. The display panel receives standard raster order RGB parallel video; the video can be cropped, down-scaled, and color corrected. The processed video data is then stored to an on-chip frame buffer. While a new image is being accumulated into a frame buffer, the previous frame of video data is then converted to the data necessary for sequential color operation, and the voltage and timing of the display's pixels are controlled so as to recreate the color and gray shade for each pixel of the processed image.

The top surface of the display panel is pixelated. Each pixel's voltage is referenced to a common electrode voltage. A series of pixel voltage pulses results in an optical PWM of the polarization of light reflecting from that pixel. The display panel generates red, green, and blue illumination control signals to control the illumination system so as to illuminate the pixels while each pixel generates the PWM optical function.

The display panel includes a 2-wire serial interface whereby a host processor can enable and shut down the display as well as customize the various features. The display panel includes an on-chip temperature sensor to automatically compensate the LC drive across the operating temperature range.

The display panel receives progressive scan raster order video data. The video may be formatted as 24-bit RGB, 4:4:4 YCbCr, 4:2:2 YCbCr. Video timing signals Vsync, Hsync, and Clock are used to instruct the display where to position the video information. The video timing signal Valid may be used to indicate which period of which line to sample as the active data. Alternately, display registers may be programmed to instruct the display to automatically sample the video data after some delay from the end of the vertical and horizontal sync timing signals.

Three RGB illumination timing signals are generated by the display panel to control a separate illumination system.

A 2-wire serial interface is used to access the display panel's control registers. The details of the serial interface are outlined in the "Serial Interface" section.

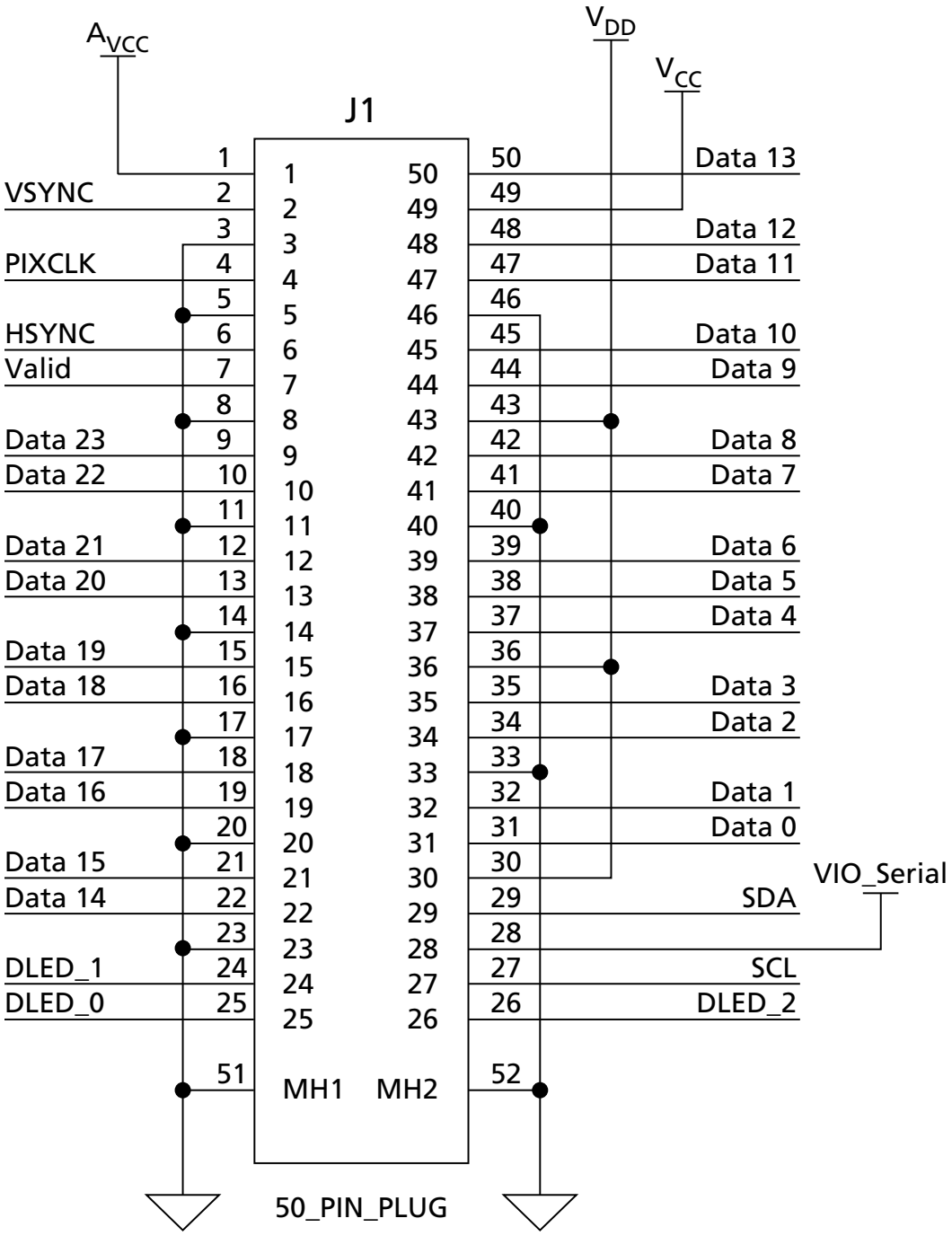
A 1.8V digital power supply powers the IC. An analog 5V power supply is used to generate the necessary analog voltages to control the liquid crystal. The signaling voltages for the serial interface are independently user selectable in the range of 1.8–3.3V and are set by the voltage applied to the VIO_Serial pin. The video data interface tolerates 1.8V–3.3V signaling.

The display panel contains a minimum of on-board bypass capacitance. The display drive system must then either provide low impedance power supplies or adequate decoupling capacitance near the display to guarantee the specified power supply conditions are met.

The display panel is interfaced through a 0.4mm pitch board-to-board connector (plug). The board-to-board connector is a 2-row connector. The connector pinout has been chosen so as to simplify the routing of the video data bus at the mating connector (receptacle), as shown in Figure 5 (page 12).

Table 4 (page 13) shows the pin assignments for the 50-pin connector.

Figure 5: Simplified Video Data Bus Routing



Pin Assignments and Descriptions

Table 4: Panel Connector Pin Assignments

Pin	Name	Type	Function
1	AV_{CC}	Power	Analog power supply (5V)
2	VSYNC	Input	Vertical synchronization signal
3	GND	Ground	Power and signal return
4	PIXCLK	Input	Pixel clock signal
5	GND	Ground	Power and signal return
6	HSYNC	Input	Horizontal synchronization signal
7	VALID	Input	Valid synchronization signal
8	GND	Ground	Power and signal return
9	DATA 23	Input	
10	DATA 22	Input	
11	GND	Ground	Power and signal return
12	DATA 21	Input	
13	DATA 20	Input	
14	GND	Ground	Power and signal return
15	DATA 19	Input	
16	DATA 18	Input	
17	GND	Ground	Power and signal return
18	DATA 17	Input	
19	DATA 16	Input	
20	GND	Ground	Power and signal return
21	DATA 15	Input	
22	DATA 14	Input	
23	GND	Ground	Power and signal return
24	DLED_1	Output	Digital illumination control pad 1
25	DLED_0	Output	Digital illumination control pad 0
26	DLED_2	Output	Digital illumination control pad 2
27	SCL	Input	Serial interface clock input
28	VIO_Serial	Power	I/O voltage supply for serial interface pins
29	SDA	Bidirectional	Serial interface data address
30	V_{DD}	Power	Core power supply (1.8V)
31	DATA 0	Input	
32	DATA 1	Input	
33	GND	Ground	Power and signal return
34	DATA 2	Input	
35	DATA 3	Input	
36	V_{DD}	Power	Core power supply (1.8V)
37	DATA 4	Input	

Table 4: Panel Connector Pin Assignments (Continued)

Pin	Name	Type	Function
38	DATA 5	Input	
39	DATA 6	Input	
40	GND	Ground	Power and signal return
41	DATA 7	Input	
42	DATA 8	Input	
43	V_{DD}	Power	Core power supply (1.8V)
44	DATA 9	Input	
45	DATA 10	Input	
46	GND	Ground	Power and signal return
47	DATA 11	Input	
48	DATA 12	Input	
49	V_{CC}	Power	Analog power supply (3.3V)
50	DATA 13	Input	

Electrical Specifications

Table 5: DC Characteristics

Symbol	Parameter	Measurement Conditions	Min	Typ	Max[3]	Unit
V_{IH_Video}	Input high voltage	For all video inputs	VIO_Video x 0.74	–	VIO_Video x 0.8	V
V_{IH_Serial}	Input high voltage	For all serial inputs	VIO_Serial x 0.74	–	VIO_Serial x 0.8	V
V_{IL_Video}	Input low voltage	For all video inputs	VIO_Video x 0.18	–	VIO_Video x 0.25	V
V_{IL_Serial}	Input low voltage	For all serial inputs	VIO_Serial x 0.18	–	VIO_Serial x 0.25	V
I_C	Input capacitance	For all inputs, 3.3V Sqr @ 27 MHz	–	tbd	tbd	pF
I_{IL}	Input leakage current	$V_I = V_{IL\_Video}$ V_{IL_Serial}	tbd	–	–	µA
I_{IH}		$V_I = V_{IH\_Video}$ V_{IH_Serial}	–	–	tbd	µA
V_{OL}	Output low voltage	I_{OL} = 1mA	tbd	–	–	µA
V_{OH}	Output high voltage	I_{OH} = –1mA	–	–	tbd	
V_{DD}	Supply voltage		1.65	1.8	1.95	V
V_{VIO_Serial}	Supply voltage	User selectable, nominally 1.8–3.3V	1.65	3.3	3.6	V
V_{CC}	Supply voltage		3.0	3.3	3.6	V
AV_{CC}	Supply voltage		4.5	5.0	5.5	V
I_{VDD}	Average panel operating supply current [1]		–	tbd	tbd	mA
I_{VCC} I_{VCC}	Average panel operating supply current[1]		–	tbd	tbd	mA
I_{VIO_Serial} I_{VIO_Video}	Average panel operating supply current[1]		–	tbd	tbd	mA
I_{AVCC}	Average panel operating supply current[1]		–	tbd	tbd	mA
I_{VDD_STBY} I_{VIO_Serial}	Average panel supply current[1]		–	tbd	–	mA
I_{VCC_STBY}	Average panel operating supply current[1, 4]		–	tbd	–	mA
$I_{VIO\_Serial\_STBY}$	Average panel supply current[1, 4]		–	tbd	–	mA
I_{AVCC_STBY}	Average panel supply current[1, 4]		–	tbd	–	

Notes:
1. Typical values at 60Hz, 960 x 540 operation with flat-field video pattern at room temperature.
2. Typical values with all inputs stopped at room temperature.
3. All MAX values measured with the corresponding maximum allowable supply voltage.

4. Average supply current of VIO_Serial is dependent on static DC current defined by internal pull-up resistors over time.
5. Worst case for this measurement is with single pixel checkerboard.

Table 6: Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{DD} to GND	–0.5	1.95	V
V_{CC} to GND	–0.5	3.6	V
VIO_Serial to GND	–0.5	3.6	V
AVCC	–0.5	5.5	V
Voltage on any Video input pin to GND	GND - 0.4	3.3 + 0.4	V
Voltage to any VIO_Serial input pin to GND	GND - 0.4	VIO_Serial + 0.4	V

Video Input Signal Timing Requirements

All video input signals must meet the timing requirements shown in Figure 6 and Table 7.

Figure 6: Video Input Signal Timing

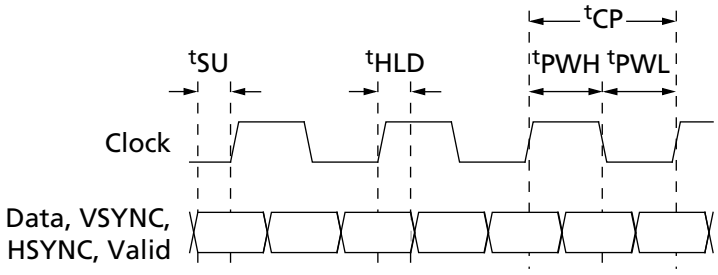


Table 7: AC Characteristics – Video Input Signal Timing

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK, rate	1/tCP	25	–	75	MHz
CLOCK, pulse width high	tPWH	40% tCP	50% tCP	60% tCP	
CLOCK, pulse width low	tPWL	40% tCP	50% tCP	60% tCP	
DATA, VSYNC, HSYNC, VALID, setup time	tSU	1.25	–	–	ns
DATA, VSYNC, HSYNC, VALID, hold time	tHLD	1.25	–	–	ns

Configuration Interface

A commonly available two-wire interface is implemented in the qHD panel. The two-wire interface requires resistor pull-ups for proper function. Both SDA and SCL are bidirectional lines, connected to VIO_Serial supply level via externally provided pull-up resistors. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the two-wire interface bus can be transferred at rates of up to 100 kb/s in the standard mode and up to 400 kb/s in the fast mode. The qHD panel is in fast mode by default. The bus does not auto-scale down to 100 kHz if there is an issue. The sizes of the resistor pull-ups are dependent on the bus speed and the load from the system on the bus interface.

Timing

The timing for the external two-wire interface is seen in Figure 7 and Table 8 (page 19). These must be adhered to for the two-wire interface to correctly function.

Figure 7: External Two-Wire Interface Timing

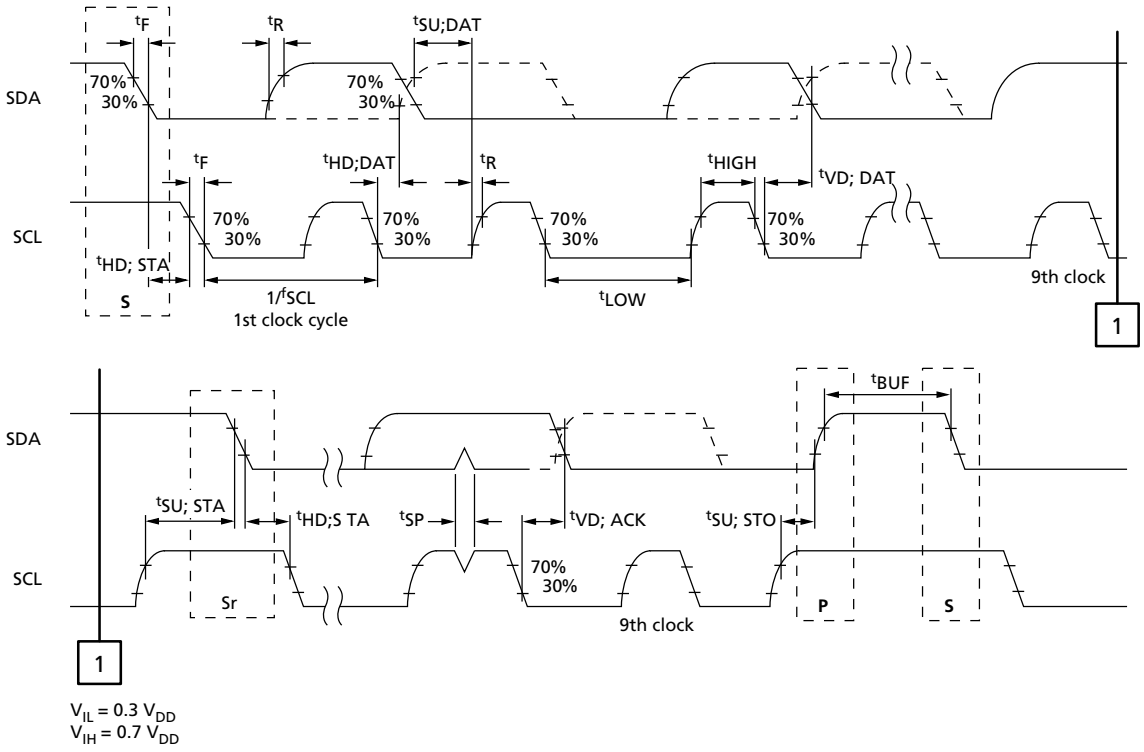


Table 8: External Two-Wire Interface Timing Specifications

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
SCL clock frequency	^{f}SCL		0	100	0	400	kHz
Hold time (and repeated) START condition	^{t}HD:STA	After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
Low period of the SCL clock	^{t}LOW		4.7	–	1.3	–	µs
High period of the SCL clock	^{t}HIGH		4.0	–	0.6	–	µs
Setup time for a repeated START condition	^{t}SU:STA		4.7	–	0.6	–	µs
Data hold time	^{t}HD:DAT		5	–	5	–	ns
Data setup time	^{t}SU:DATA		250	–	100	–	ns
Rise time of both SDA and SCL signals	^{t}r		–	1000	20 + 0.1Cb	300	ns
Fall time of both SDA and SCL signals	^{t}f		–	300	20 + 0.1Cb	300	ns
Setup time for STOP condition	^{t}SU:STO		4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	^{t}BUF		4.7	–	1.3	–	µs
Capacitive load for each bus line (depends on load and frequency)	Cb		–	400	–	400	pF
Data valid time	^{t}VD:DAT		–	3.45	–	0.9	µs
Data valid acknowledge time	^{t}VD:ACK		–	3.45	–	0.9	µs
Pulse width of spikes that must be supressed by the input filter	^{t}SP		n/a	n/a	0	50	ns

Protocol

The external two-wire interface follows the simple serial protocol. The qHD panel is always considered a slave in the system and requires a clock to be provided to it for all two-wire interface transactions. A start condition is generated through the use of pulling down the SDA line while SCL is still high. The next 7 bits are the device address of the device the issuing device is looking to communicate with. For the qHD panel, the external interface device address is 0111 1110[R/!W]. The 8th bit sent is the R/W bit, where if a read is requested then the bit should be kept high, and if a write is requested the line is pulled down to a low-level signal. The 9th bit is the acknowledgment bit from the addressed device. If the addressed device receives its address and is not busy at that time it will respond by pulling the SDA line low and therefore signaling an acknowledgment. The device issuing the request is still required to provide the clock pulse (SCL). If an acknowledgment is detected by the issuing device, then the rest of the message can be sent.

Figure 8 and Figure 9 are two-wire interface protocol waveforms showing a single-byte READ and single-byte READ transaction for the qHD panel using the two-wire interface protocol. For each of these transactions, a START signal must be presented first. This is when the SDA line is pulled low while the SCL line is kept high. The first byte sent is always the device address for the qHD panel's external two-wire interface (0111 110[R/! W]) followed by the R/W bit. An acknowledge (ACK) is returned from the receiving device after each byte sent by pulling the SDA line low for one clock. The clock is still provided by the master device, which is never the qHD panel display. The second byte sent in both the write and read transactions is the qHD panel's 8-bit register address that will be read or written. After the register address is sent, the byte to be written or read is sent. In the case of the write, the master keeps control of the bus and delivers the byte to be written. In the read case, the master releases the bus and the slave takes control and sends the data byte to be read back to the master.

Figure 8: Two-Wire Interface: Single-byte WRITE Transaction

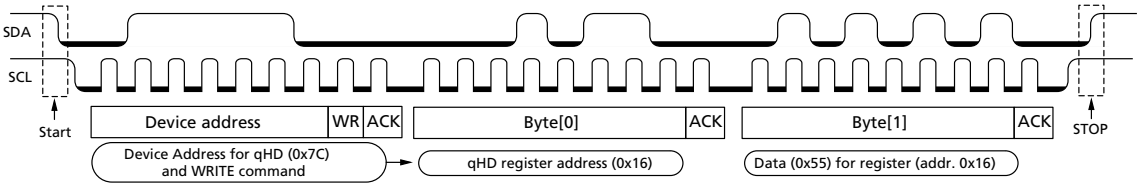
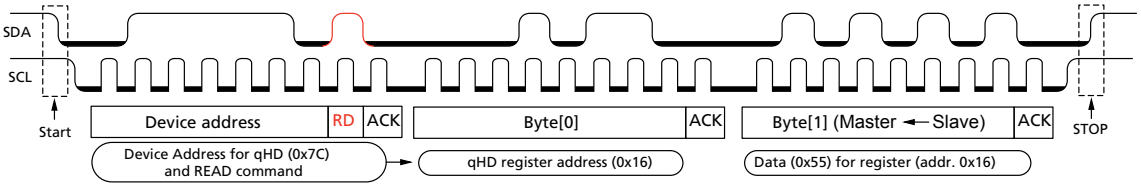


Figure 9: Two-Wire Interface: Single-byte READ Transaction



In a multi-byte write transaction the master provides to the qHD panel's external two-wire interface one or more bytes of data to be written to the address specified. The address is auto-incremented for each byte written. During a multi-byte read transaction, once the register address is sent by the master, the slave (the qHD panel) now takes control of the bus and transmits one or more bytes of data from the address provided earlier in the transaction. The address is auto-incremented for each byte read, similar to a write transaction. During a read, the master provides the acknowledge pulse.

Figure 10: Two-Wire Interface: Multi-byte WRITE Transaction

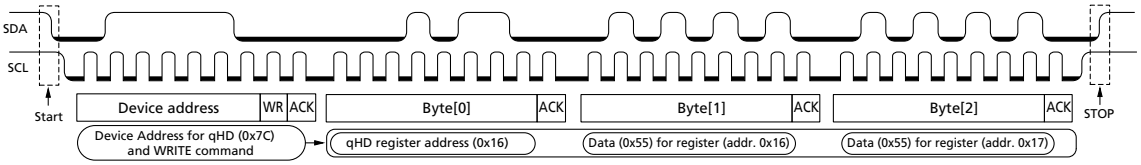
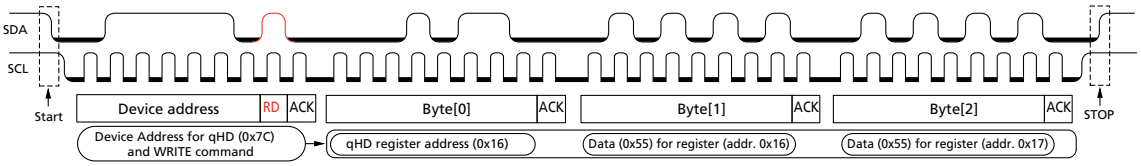


Figure 11: Two-Wire Interface: Multi-byte READ Transaction



Function

The external interface is used to access the configuration register space for the qHD panel. It is capable of reading and writing the register space while in sleep mode as long as power is still applied to the display. The external two-wire interface is a slave device with a default slave address of 0111 110[R/!W]. The two-wire interface supports both 100 kHz and 400 kHz bus speeds and anywhere in between. The external two-wire interface requires external pull-ups on the SDA and SCL lines for proper functionality. The external two-wire interface does not support clock-stretching at this time.

Control Sequence Requirements

Timing/sequence requirements must be met during power-up and power-down of the display panel. The required control sequence of the display panel is shown in Figure 12, and timing requirements are given in Table 9 (page 23).

The power supplies may be enabled in any order. After the voltage supplies (V_{DD}, VIO_Serial) are present and in specification, the NRESET input is high and the CLOCK input is toggling, the display panel will load default register values from nonvolatile memory to RAM for a time period of ^{t}PWRUP. During this time period, the serial interface is ignored. The CLOCK must continue to toggle during a time period of ^{t}POCLK from the end of the ^{t}PWRUP time period. After the ^{t}POCLK time period, the CLOCK input may continue to toggle or it may be disabled.

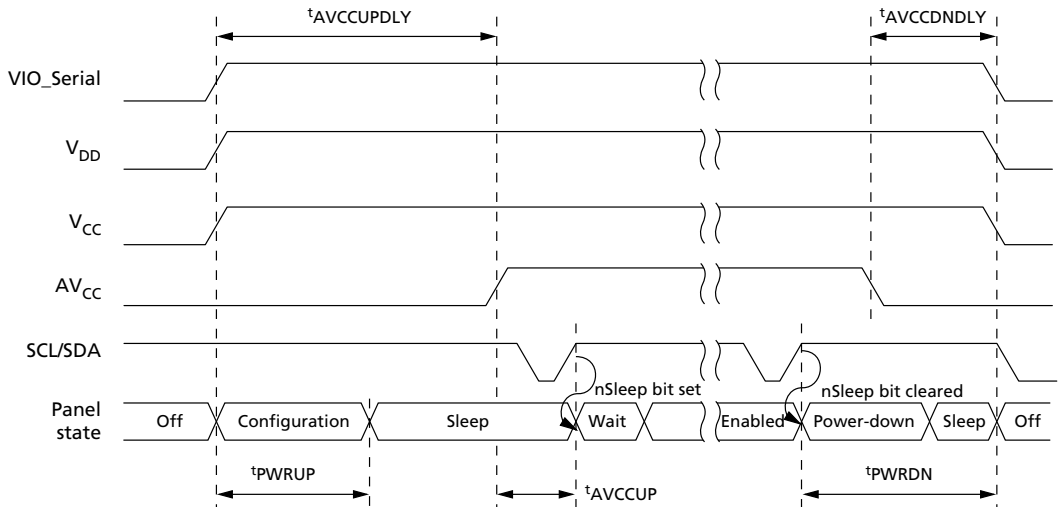
After the ^{t}PWRUP period, the display panel will be in the Sleep state and the serial interface is active. The display panel is enabled by using the serial interface to set the nSleep bit of the video sleep register. The V_{CC} power supply must be present for a time period of ^{t}VCCUP before the nSleep bit is set. If the V_{CC} power supply is not present when the display is enabled, no image will be driven until V_{CC} is detected. The nSleep bit may be set without the clock present, but the display will not be enabled until both the clock and a valid video signal are present.

For correct panel operation, the control registers must be correctly programmed according to the input video signals and desired display operation. If the default values are incorrect or undesirable, the serial interface is used to program the appropriate settings prior to enabling the display panel.

Once the display panel has been enabled, it must be disabled using the specific sequence shown in Figure 12. The shutdown sequence is required to avoid damage to the display and to maintain performance. As shown in Figure 12, the shutdown procedure requires using the serial interface to clear the nSleep bit putting the display into sleep mode. For the time period ^{t}PWRDN after the nSleep bit has been cleared, the power supplies and CLOCK inputs must remain present. The clocks and power supplies to the display can be removed anytime after ^{t}PWRDN has elapsed to complete a successful shutdown of the display.

While in sleep mode, with clock and power supplies present, the configuration register state of the display is maintained. However, the incoming video data is ignored. This configuration state retention allows the display to cycle in and out of sleep mode without reconfiguration. If the display is shutdown by removing the clock and power supplies after minimum sleep duration of ^{t}PWRDN, the device will require reconfiguration.

Figure 12: Power-Up and Power-Down Control Sequence



Note: 1. SEN is relative to the VIO_Serial supply.

Table 9: AC Characteristics – Control Sequence Timing

Parameter	Symbol	Min	Typ	Max	Unit
Time from last valid power supply until display is ready for use	tCONFIG	23	–	–	ms
Time from last valid power supply until A_{VCC} can be applied	tAVCCUPDLY	400	–	–	µs
Time from valid A_{VCC} power supply to enable of display using nSleep bit	tAVCCUP	1	–	–	ms
Time from AV_{CC} power down to V_{CC} power down	tAVCCDNDLY	200	–	–	µs
Time from disable of display panel using the nSleep bit to removal of V_{CC}, V_{DD}, and VIO_Serial	tPWRDN	1500	–	–	µs

Video Input Interface

The display panel provides a universal parallel video interface. Video data may be formatted as RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2. The display panel's sampling of video input data can be configured to any of three formats. The video input data bus would then be driven with the appropriate data signals as shown in the Table 10.

Table 10: Signal Assignments for Video Data Format Modes

Pin	RGB 4:4:4	YCbCr 4:4:4	YCbCr 4:2:2
DATA 0	RED0	Y0	Y0
DATA 1	RED1	Y1	Y1
DATA 2	RED2	Y2	Y2
DATA 3	RED3	Y3	Y3
DATA 4	RED4	Y4	Y4
DATA 5	RED5	Y5	Y5
DATA 6	RED6	Y6	Y6
DATA 7	RED7	Y7	Y7
DATA 8	GREEN0	Cb0	Cb0/Cr0
DATA 9	GREEN1	Cb1	Cb1/Cr1
DATA 10	GREEN2	Cb2	Cb2/Cr2
DATA 11	GREEN3	Cb3	Cb3/Cr3
DATA 12	GREEN4	Cb4	Cb4/Cr4
DATA 13	GREEN5	Cb5	Cb5/Cr5
DATA 14	GREEN6	Cb6	Cb6/Cr6
DATA 15	GREEN7	Cb7	Cb7/Cr7
DATA 16	BLUE0	Cr0	GND
DATA 17	BLUE1	Cr1	GND
DATA 18	BLUE2	Cr2	GND
DATA 19	BLUE3	Cr3	GND
DATA 20	BLUE4	Cr4	GND
DATA 21	BLUE5	Cr5	GND
DATA 22	BLUE6	Cr6	GND
DATA 23	BLUE7	Cr7	GND

The display panel's control registers can be set to specify the desired operating mode. In the first mode, the state of the VALID signal is used to indicate on which clocks the video data is to be sampled. In the second mode, the display panel control registers are programmed to instruct the display panel to automatically sample video at fixed times after the assertion of the HSYNC and VSYNC signals. Figure 13 (page 25), Figure 14 (page 25), and Table 11 (page 26) provide the requirements for the video input format.

Figure 13: Video Input Vertical Timing

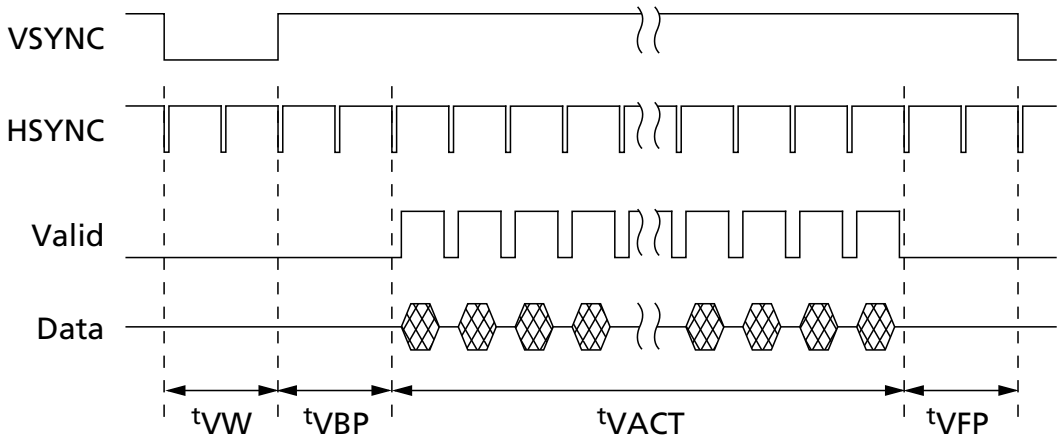


Figure 14: Video Input Horizontal Timing

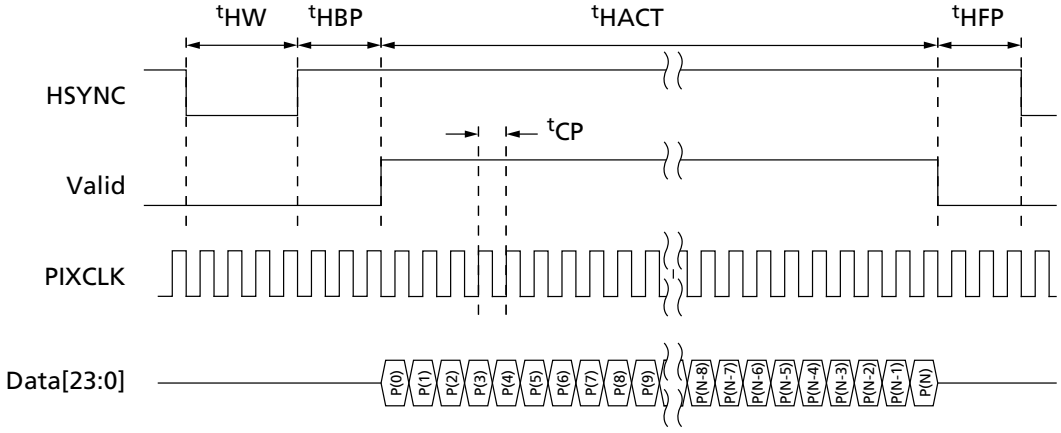


Table 11: AC Characteristics – Video Format Timing[1]

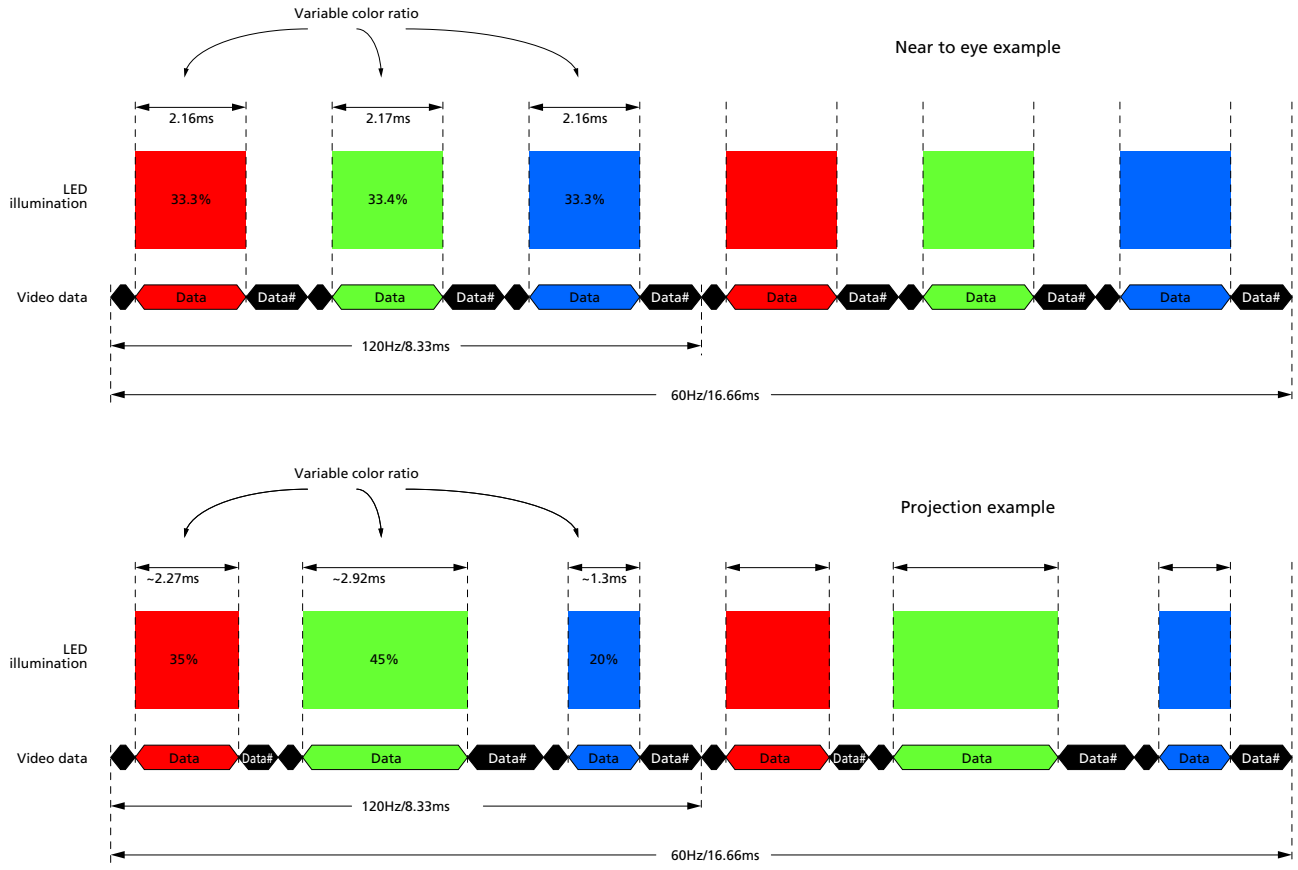
Parameter	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	^{t}VF	47	60	63	Hz
VSYNC, total lines	^{t}VTOT = ^{t}VBLK + ^{t}VACT	282	tbd	1088	Line
VSYNC, active lines	^{t}VACT	270	540	768	Line
VSYNC, blanking	^{t}VBLK = ^{t}VFP + ^{t}VW + ^{t}VBP	12	tbd	200	Line
VSYNC, front porch	^{t}VFP	5	tbd	94	Line
VSYNC, pulse width	^{t}VW	3	tbd	94	Line
VSYNC, back porch	^{t}VBP	3	tbd	94	Line
HSYNC, total clocks	^{t}HTOT = ^{t}HBLK + ^{t}HACT	524	tbd	1392	Clock
HSYNC, active clocks	^{t}HACT	480	tbd	1368	Clock
HSYNC, blanking	^{t}HBLK = ^{t}HFP + ^{t}HW + ^{t}HBP	24	tbd	512	Clock
HSYNC, front porch	^{t}HFP	12	tbd	512	Clock
HSYNC, pulse width	^{t}HW	4	tbd	128	Clock
HSYNC, back porch	^{t}HBP	8	tbd	512	Clock
CLOCK, rate	1/^{t}CP	25	tbd	75	MHz

Note: 1. All minimum and maximum timing specifications must be met simultaneously.

Duty Cycle

The qHD display panel shows red, green, and blue images for variable lengths of time as dictated by temperature and register programming. While a color image is displayed, the corresponding color LED command signal is generated in order to maintain alignment of the displayed data and illumination source. This operation is shown Figure 15 along with the resulting LED output signals. The display panel default operation is set for a typical projection application, with color ratios defined as Red = 35%, Green = 45%, and Blue = 20%.

Figure 15: LED Duty Cycle



Configuration Registers

The configuration registers are set at power-up by the integrated EEPROM; subsequently, they can be read and written with the 2-wire serial interface. Any register not described is considered Reserved and is not intended for customer use. Altering Reserved registers is not supported and may result in erroneous operation.

Reserved Register with Default Settings

Table 12: Register Index 00h (Register is Read Only)

Bit							
7	6	5	4	3	2	1	0
RES							
00h							

Video Mode Register with Default Settings

Table 13: Register Index 01h (Register is RW)

Bit							
7	6	5	4	3	2	1	0
CSpaceSel	ChannelMap			DataChannel		DataSequence	
0	000			00		00	

Notes:
1. **CSpaceSel:** Color Space Select, 0 = RGB, 1 = YCbCr
2. **ChannelMap:** Select mapping of data channel to color information, dependent on the DataChannel setting according to the following table.

Table 14: Mapping Data Channel to Color Information

Channel Map	24-bit RGB			24-bit YCbCr			16-bit YCbCr		
	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]
1h	Green	Red	Blue	Cb	Y	Cr	–	Y	Cb/Cr
0h	Blue	Green	Red	Cr	Cb	Y	–	Cb/Cr	Y
2h	Red	Blue	Green	Y	Cr	Cb	Cb/Cr	Y	–
3h	Red	Green	Blue	Y	Cb	Cr	Y	Cb/Cr	–
4h	Green	Blue	Red	Cb	Cr	Y	Cb/Cr	–	Y
5h	Blue	Red	Green	Cr	Y	Cb	Y	–	Cb/Cr

Notes:
1. **Data Channel:** 00 = 24-bit data interface, 01 = 16-bit data interface
2. **DataSequence:** Data Sequence, 00 for 24-bit RGB or YCbCr interface. Selects sequence of color information for 16-bit YCbCr interface mode according to the following table.

Table 15: Data Sequence of Color Information for 16-bit Interface

Data Sequence	16-bit YCbCr
00	[Y0Cb] [Y1Cr]
01	[Y0Cr] [Y1Cb]
10	–
11	–

Video Configuration Register with Default Settings

Table 16: Register Index 02h (Register is RW)

Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VPol	HPol	ValidPol	RES	RES	RES	SyncMode	
1	1	0	0	0	0	00	

Notes:
1. **VPol:** Vertical sync polarity; 0 = ACTIVE HIGH, 1 = ACTIVE LOW
2. **HPol:** Horizontal sync polarity; 0 = ACTIVE HIGH, 1 = ACTIVE LOW
3. **ValidPol:** Valid input polarity; 0 = ACTIVE HIGH, 1 = ACTIVE LOW
4. **SyncMode:**
   - 00 = Use HSYNC, VSYNC, and VALID inputs for video timing
   - 01 = Use HYSNC and VSYNC inputs; VALID timing specified from valid delay registers
   - 10 = Reserved
   - 11 = Reserved

Scaling Coefficient Registers with Default Settings

Table 17: Register Index 04h–0Bh (Registers are RW)

Index	Default	Bit							
		7	6	5	4	3	2	1	0
04h	00h	RES							
05h	00h	RES							
06h	02h	RES		VScaleCycle[9:8]		RES		VscaleStep[10:8]	
07h	00h	VScaleStep[7:0]							
08h	01h	VScaleCycle[7:0]							
09h	02h	RES		HScaleCycle[9:8]		RES		HScaleStep[10:8]	
0Ah	00h	HScaleStep[7:0]							
0Bh	01h	HScaleCycle[7:0]							

Notes:
1. **HScaleStep:** Horizontal scaling repeat count
2. **HScaleCycle:** Horizontal scaling repeat count
3. **VScaleStep:** Vertical scaling coefficient
4. **VScaleCycle:** Vertical scaling repeat count

Vertical Valid Delay Register with Default Settings

Table 18: Register Index 0Ch (Register is RW)

Bit							
7	6	5	4	3	2	1	0
VVldDelay [7:0]							
00h							

Note:
1. **VVldDelay:** Vertical valid delay.

Vertical Valid Delay Offset Register with Default Settings

Table 19: Register Index 0Dh (Register is RW)

Bit							
7	6	5	4	3	2	1	0
RES						HVldDelay[9:8]	
00						00	

Horizontal Valid Delay Register with Default Settings

Table 20: Register Index 0Eh (Register is RW)

Bit							
7	6	5	4	3	2	1	0
HVldDelay[7:0]							
00h							

Note: 1. **HVldDelay:** Horizontal valid delay; the delay (in clocks) from horizontal valid assertion to sampled video when using valid input; otherwise, delay from Hsync assetion to sampled video - 2.

Color Space Gain Registers with Default Settings

Table 21: Register Index 0Fh–17h (Registers are RW)

Index	Default	Bit							
		7	6	5	4	3	2	1	0
0Fh	00h	ColorSpace11							
10h	00h	ColorSpace12							
11h	00h	ColorSpace13							
12h	00h	ColorSpace21							
13h	00h	ColorSpace22							
14h	00h	ColorSpace23							
15h	00h	ColorSpace31							
16h	00h	ColorSpace32							
17h	00h	ColorSpace33							

Color Space Offset Registers with Default Settings

Table 22: Register Index 18h–1Ah (Registers are RW)

Index	Default	Bit							
		7	6	5	4	3	2	1	0
18h	00h	ColorOffset1							
19h	00h	ColorOffset2							
1Ah	00h	ColorOffset3							

The CSpaceSel bit of the Video Mode register (register 01h, bit 7) determines the base color space transformation for RGB or YCrCb data as shown in Figure 16, part (a) for RGB and part (b) for YCrCb. The coefficients for the selected RGB or YCrCb transformation are highlighted in yellow. The base color space transformation may be modified using the 8-bit signed number color space adjustment values from configuration registers ColorSpace11–ColorSpace33 (12h–1Ah) and ColorOffset1–ColorOffset3 (1Bh–1Dh), highlighted in blue. A value of 0 for CSpaceSel selects the base transformation in Figure 16(a) used for RGB input data, while a value of 1 for CSpaceSel selects the base transformation in Figure 16(b) for Cr input data.

Figure 16: Color Space Gain and Offset Selection

$$\begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128 + cs_{11} & 0 + cs_{12} & 0 + cs_{13} \\ 0 + cs_{21} & 128 + cs_{22} & 0 + cs_{23} \\ 0 + cs_{31} & 0 + cs_{32} & 128 + cs_{33} \end{bmatrix} \times \begin{bmatrix} R_1 + 0_1 \\ G_1 + 0_2 \\ B_1 + 0_3 \end{bmatrix}$$

(a)

$$\begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128 + cs_{11} & 0 + cs_{12} & 175 + cs_{13} \\ 128 + cs_{21} & -42 + cs_{22} & -90 + cs_{23} \\ 128 + cs_{31} & 222 + cs_{32} & 0 + cs_{33} \end{bmatrix} \times \begin{bmatrix} Y_1 + 0_1 \\ Cb_1 - 128 + 0_2 \\ Cr_1 - 128 + 0_3 \end{bmatrix}$$

(b)

Gamma Register with Default Settings

Table 23: Register Index 54h (Register is RW)

Bit							
7	6	5	4	3	2	1	0
RES	DLEDInv	DLEDEn	RES	GammaVal			
0	0	0	0	29h			

Notes:
1. **DLEDInv:** 0 = ACTIVE HIGH digital LED outputs, 1 = ACTIVE LOW digital LED outputs
2. **DLEDEn:** 0 = Disable digital LED outputs, 1 = Enable Digital LED outputs
3. **GammaVal:** Selected display gamma; values shown the following table.

Table 24: Display Gamma Values

GammaVal	Display Gamma	GammaVal	Display Gamma
0h	1.0	8h	2.0
1h	1.2	9h	2.1
2h	1.4	Ah	2.2
3h	1.5	Bh	2.3
4h	1.6	Ch	2.4
5h	1.7	Dh	2.6
6h	1.8	Eh	2.8
7h	1.9	Fh	3.0

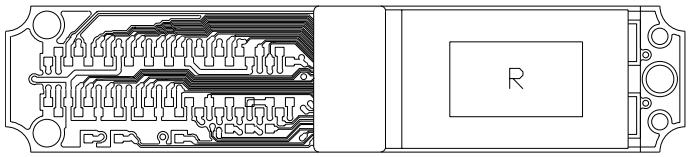
Video Sleep Register with Default Settings

Table 25: Register Index 55h

Bit							
7	6	5	4	3	2	1	0
RES							nsleep_mode
000			1	00		0	

Note: 1. • **nsleep_mode:** Sleep mode enable; ACTIVE LOW

Figure 17: Display Orientation with VFlip = 0 and HFlip = 0



Color Ratio Registers with Default Settings

Table 26: Register Index 6Ah–6Ch (Registers are RW)

Index	Default	Bit							
		7	6	5	4	3	2	1	0
6Ah	55h	RedRatio							
6Bh	56h	GreenRatio							
6Ch	55h	BlueRatio							

Notes:
1. **RedRatio:** Ratio out of 256d time periods for red display time. (55h = 85d = ratio for red 33.2%)
2. **GreenRatio:** Ratio out of 256d time periods for green ramp time. (56h = 86d = ratio for green 33.6%)
3. **BlueRatio:** Ratio out of 256d time periods for blue ramp time. (55h = 85d = ratio for blue 33.2%)

These registers determine the proportion of available illumination time used for each color, which allows the system designer to optimize the efficiency of the illumination system. The sum of the red, green, and blue ratios should be 256d and may not exceed 256d.

Temperature Measurement Register

Table 27: Register Index 92h (Register is Read Only)

Bit							
7	6	5	4	3	2	1	0
ChipTemp[7:0]							
FFh							

Note:
1. **ChipTemp:** Chip temperature measurement; the on-chip temperature sensor records temperature as an 8-bit value.

DISPORIENT Register

Table 28: Register Index D0h

Bit							
7	6	5	4	3	2	1	0
RES						VFlip	HFlip
000000						0	0

Note: 1. • **VFlip:** 0 = Disable display vertical flip mode; 1 = Enable display vertical flip mode
• **HFlip:** 0 = Disable display horizontal flip mode; 1 = Enable display horizontal flip mode

ID Code Registers with Default Settings

Table 29: Register Index FCh–FEh (Registers are Read Only)

Index	Bit							
	7	6	5	4	3	2	1	0
FCh	IDCode[7:0]							
EDh	IDCode[15:8]							
FEh	IDCode[23:16]							

Note: 1. **IDCode:**This 24-bit code is a unique serial number for each display device.

Revision History

Rev. B, Preliminary – 06/11

- Features: Updated reflectivity from 60% to 58%; updated package dimensions from 27.0mm x 5.8mm x 2.6mm to 27.0mm x 5.8mm x 2.7mm in Table 1.
- Optical Specification:
  - Added the following comment: ". . . for best performance, the polarizing optics must be aligned with the columns of the display."
  - Updated the fill factor from 87.7% to 86% typical; changed reflectivity from 60% to 58% typical; removed bright pixels specification row in Table 3.
- Duty Cycle:
  - Moved description to Configuration Registers.
  - Updated the LED Duty Cycle graphic and added the following description: "The display panel default operation is set for a typical projection application, with color ratios defined as Red = 35%, Green = 45%, and Blue = 20%."
- Mechanical Specifications:
  - Clarified that the diameter of the locating holes is 1.10mm.
  - Correct Molex connector part number to 502430-5010.
  - Updated package diagrams
- Pin Assignments and Descriptions:
  - Clarified function description of the following pins: VSYNC, PIXCLK, HSYNC, VALID, VIO_Serial
- Electrical Specifications
  - Updated DC Characteristics
  - Added AVCC to GND row to Absolute Maximum Ratings
- Control Sequence Requirements
  - Updated Power-Up and Power-Down Control Sequence figure
  - Updated AC Characteristics – Control Sequence Timing
  - Removed description following table and removed Sleep State Control Sequence figure
- Video Input Interface
  - Updated CLOCK, rate MAX value from 512 to 75
- Updated Register Index 00h (Register is Read Only) table in Reserved Register with Default Settings
- Updated Bit 0 from 000 to 001 in Video Mode Register with Default Settings
- Updated Index values in Register Index 0Fh–17h (Registers are RW) table in Color Space Gain Registers with Default Settings
- Updated Index values in Register Index 18h–1Ah (Registers are RW) table in Color Space Offset Registers with Default Settings
- Updated Index values in Register Index FCh–FEh (Registers are Read Only)
- Updated Index values in Register Index 6Ah–6Ch (Registers are RW)
- Updated Bit 5 from 0 to 1 in Register Index 54h (Register is RW) table in Gamma Register with Default Settings

- Video Sleep Register with Default Settings
  - Updated Bits 3:0 to be 00 in Register Index 55h table
  - Updated Display Orientation with FVlip = 0 and HFlip = 0 graphic
- Color Ratio Registers with Default Settings
  - Updated Index and Default values in Register Index 6A–6Ch (Registers are RW) table
  - Updated value in notes
- Added clarification notes to Temperature Measurement Register
- Updated Index values in Register Index FC–FEh (Registers are Read Only) table in ID Code Registers with Default Settings

Rev. A, Preliminary – 03/11

- Initial release.

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.